IN THE CLAIMS

1. (Currently Amended) A semiconductor device, comprising:

a substrate including a contact pad;

a solder bump formed on said contact pad; [[and]]

[[an]] a first absorption layer disposed between said contact pad and said solder bump, said first absorption layer having a thickness that is configured to substantially stop alpha particles of at least 5.4 MeV [[.0]] ; and

a second solder bump formed over a second absorption layer, wherein said first absorption layer and said second absorption layer are laterally isolated from each other by a spacing of approximately 1-100 μm.

2. (Currently Amended) The semiconductor device of claim 1, wherein each of said first and second absorption [[layer]] layers comprises at least one of copper, nickel, chromium, tungsten, gold, silver, platinum, tantalum and a compound thereof.

3. (Currently Amended) The semiconductor device of claim 1, wherein each of said first and second absorption [[layer]] layers comprises two or more sub-layers.

4. (Currently Amended) The semiconductor device of claim 1, wherein each of said first and second absorption [[layer]] layers is adapted to reduce passage of alpha particles to a rate less than 0.001 alpha particles/cm^2 an hour.

5. (Currently Amended) The semiconductor device of claim 1, wherein each of said first and second absorption [[layer]] layers laterally extends beyond said solder bump.

6. (Currently Amended) The semiconductor device of claim 4, further comprising a passivation layer covering a peripheral portion of each of said first and second absorption [[layer]] layers.

7. (Cancel)

8. (Currently Amended) The semiconductor device of claim [[8]] 1, wherein said spacing is filled with a dielectric material.

9. (Currently Amended) The semiconductor device of claim 1, wherein a thickness of each of said first and second absorption [[layer]] layers is in the range of approximately 1-10 μm.

10. (Currently Amended) The semiconductor device of claim 1, wherein an intrinsic alpha particle emission rate of each of said first and second absorption [[layer]] layers is less than 0.001 alpha particles/cm^2 an hour.

11. (Currently Amended) A semiconductor device, comprising:

a substrate including [[a contact pad]] a plurality of contact pads;

[[a solder bump formed on said contact pad]] a plurality of solder bumps, each of said solder bums formed on one of said plurality of contact pads; and

[[an underbump metallization disposed between said contact pad and said solder bump, a plurality of underbump metallization layers, each of said underbump metallization layers substantially preventing diffusion of solder bump material into said substrate and providing adhesion of each of said solder [[bump]] bumps to said substrate, wherein each of said underbump metallization layers has a thickness sufficient to stop alpha particles of approximately 5.4 MeV and adjacent underbump metallization layers being laterally isolated from each other by a spacing of 1-100 μm.

12. (Currently Amended) The semiconductor device of claim 11, wherein an intrinsic alpha particle emission rate of each of said underbump metallization layers is less than 0.001 alpha particles/cm^2 an hour

13. (Currently Amended) The semiconductor device of claim 11, wherein a thickness of each of said underbump metallization layers is in the range of approximately 1-10 μm.

14. (Currently Amended) The semiconductor device of claim 11, wherein each of said underbump metallization layers comprises an absorption layer having a thickness of approximately 1 μm or more.

15. (Original) The semiconductor device of claim 14, wherein said absorption layer comprises at least one of copper, nickel, tungsten, gold, silver, platinum, tantalum and any compound thereof.

16. (Currently Amended) The semiconductor device of claim 11, wherein a lateral extension of each of said underbump metallization layers is larger than a lateral extension of said solder bump.

17. (Original) The semiconductor device of claim 14, wherein a thickness of said absorption layer is in the range of approximately 1-10 μm.

18. (Currently Amended) The semiconductor device of claim 11, wherein a peripheral portion of each of said underbump metallization layers is coated with a passivation layer.

19. (Currently Amended) A semiconductor device, comprising:

a substrate including a functional element;

a first and a second multilayer metal stack formed over said substrate, wherein each of said first and second multilayer metal [[stack]] stacks has an intrinsic alpha particle emission rate of less than 0.001 alpha particles/cm^2 an hour and a thickness of 1 μm and more; and

a first and a second solder bump formed on said first and second multilayer metal [[stack]] stacks, respectively, such that said first and second multilayer stacks are laterally isolated from each other by a spacing of 1-100 μm.

20. (Currently Amended) The semiconductor device of claim 19, wherein each of said first and second multilayer metal [[stack]] stacks laterally extends beyond said respective solder bump.

21. (Currently Amended) The semiconductor device of claim 19, further comprising a passivation layer covering a peripheral portion of each of said multilayer metal [[stack]] stacks.

22. (Currently Amended) The semiconductor device of claim 19, wherein each of said [[multiplayer metal stack]] first and second multilayer metal stacks comprises at least one of copper, nickel, tungsten, gold, silver, platinum, tantalum and any compound thereof.

23. (Withdrawn) A method of forming a soft error reduced semiconductor device, the method comprising:

providing a substrate having formed thereon a circuit element;

forming a contact pad over said substrate;

forming an electrically conductive absorption layer over said contact pad with a predefined thickness allowing the stoppage of alpha particles with an energy of approximately 5.4 MeV; and

forming a solder bump over said absorption layer.

24. (Withdrawn) The method of claim 23, wherein forming said absorption layer comprises depositing said absorption layer and controlling at least one process parameter to

obtain said predefined thickness.

25. (Withdrawn) The method of claim 23, further comprising forming at least one further metal layer adjacent to said absorption layer.

26. (Withdrawn) The method of claim 25, wherein a total thickness of said further metal layer and said absorption layer is in the range of approximately 1-10μm.

27. (Withdrawn) The method of claim 23, wherein said predefined thickness of said absorption layer is in the range of approximately 1-10μm.

28. (Withdrawn) The method of claim 23, further comprising forming a second solder bump over said absorption layer, and forming a trench between said solder bump and said second solder bump to electrically insulate said solder bump and said second solder bump.

29. (Withdrawn) The method of claim 28, wherein a width of said trench is in the range of approximately 1-100 μm.